

### In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1           1.       (Currently Amended) A data processing apparatus  
2 comprising:

3           a register file comprising a plurality of registers, each of  
4 said plurality of registers having a corresponding register number;

5           a first functional unit group connected to said register file  
6 and including a plurality of first functional units each having an  
7 output and further including an output multiplexer having a  
8 plurality of inputs receiving respective outputs of said first  
9 functional units and an output, said first functional unit group  
10 responsive to an instruction to

11           receive data from one of said plurality of registers  
12 corresponding to an instruction-specified first operand  
13 register number at an operand input,

14           operate on said received data employing an instruction-  
15 specified one of said first functional units, and

16           select said output of said instruction-specified one of  
17 said first functional units via said output multiplexer, and

18           output data from said output of said output multiplexer to  
19 one of said plurality of registers corresponding to an  
20 instruction-specified first destination register number from an  
21 output;

22           a second functional unit group connected to said register file  
23 and including a plurality of second functional units each having an  
24 output and further including an output multiplexer having a  
25 plurality of inputs receiving respective outputs of said second  
26 functional units and an output, said second functional unit group  
27 responsive to an instruction to

28           receive data from one of said plurality of registers  
29           corresponding to an instruction-specified second operand  
30           register number at an operand input,  
31           operate on said received data employing an instruction-  
32           specified one of said second functional units, and  
33           select said output of said instruction-specified one of  
34           said second functional units via said output multiplexer, and  
35           output data from said output of said output multiplexer to  
36           one of said plurality of registers corresponding to an  
37           instruction-specified second destination register number from  
38           an output;  
39           a first comparator receiving an indication of said first  
40           operand register number of a current instruction and an indication  
41           of said second destination register number of an immediately  
42           preceding instruction, said first comparator indicating whether  
43           said first operand register number of said current instruction  
44           matches said second destination register number of said immediately  
45           preceding instruction; and  
46           a first register file bypass multiplexer connected to said  
47           register file, said first functional unit group, said second  
48           functional unit group and said first comparator, said first  
49           register file bypass multiplexer having a first input receiving  
50           data from said register corresponding to said first operand  
51           register number of said current instruction, a second input  
52           connected to said output of said second functional unit group and  
53           an output supplying an operand to said operand input of said first  
54           functional unit group, said first multiplexer selecting said data  
55           from said register corresponding to said first operand number of  
56           said current instruction if said first comparator fails to indicate  
57           a match and selecting said output of said second functional unit  
58           group if said first comparator indicates a match;

59        said first functional units of said first functional unit  
60 group and said second functional units of said second functional  
61 unit group selected whereby functions often executed simultaneously  
62 within the same instruction cycle have corresponding functional  
63 units placed in different functional unit groups and functions  
64 which are not often executed together within the same instruction  
65 cycle have corresponding functional units placed in the same  
66 functional unit group.

1        2. (Previously Amended) The data processing apparatus of  
2 claim 1, wherein said register file, said first functional unit  
3 group, said second functional unit group, said first comparator and  
4 said first register file bypass multiplexer operate according to an  
5 instruction pipeline comprising:

6        a first pipeline stage consisting of a register read operation  
7 from said register file to provide operands for a selected  
8 functional unit of said first and second functional unit groups and  
9 a first half of operation of said selected functional unit of said  
10 first and said second functional unit groups, and

11        a second pipeline stage consisting of a second half of  
12 operation of said selected functional unit of said first and said  
13 second functional unit groups and a register write operation to  
14 said register file of results of operation of said selected  
15 functional unit of said first and second functional unit groups,

16        wherein the sum of the time of said register read operation  
17 and said register write operation equals approximately the sum of  
18 the time of said first and second halves of operation of a slowest  
19 of said functional units of said first and second functional unit  
20 groups.

1        3. (Previously Amended) The data processing apparatus of  
2 claim 1, further comprising an output register having an input

3 connected to said output of said second functional unit group and  
4 an output connected to said register file for temporarily storing  
5 said output of said second functional unit group prior to storing  
6 in said register corresponding to said second destination register  
7 number,

8 wherein said first comparator further receives an indication  
9 of said second destination register number of a second preceding  
10 instruction, said first comparator further indicating whether said  
11 first operand register number of said current instruction matches  
12 said second destination register number of said second preceding  
13 instruction, and

14 wherein said multiplexer further has a third input connected  
15 to said output register output, said multiplexer selecting said  
16 output register output if said first comparator indicates a match.

4. (Canceled)

1 5. (Previously Amended) The data processing apparatus of  
2 claim 1, said first comparator further receiving an indication of  
3 said first destination register of said immediately preceding  
4 instruction, said first comparator further indicating whether said  
5 first operand register number of said current instruction matches  
6 said first destination register number of said immediately  
7 preceding instruction, said first multiplexer further having a  
8 third input connected to said output of said first functional unit  
9 group, and said first multiplexer selecting said ~~first~~ output of  
10 said first functional unit group if said first comparator indicates  
11 a match.

1 6. (Previously Amended) The data processing apparatus of  
2 claim 1, said first functional unit group further responsive to an  
3 instruction to receive data from one of said plurality of registers

4 corresponding to an instruction-specified third operand register  
5 number at an operand input,  
6 said apparatus further comprising:  
7 a second comparator receiving an indication of said third  
8 operand register number of a current instruction and an indication  
9 of said second destination register number of said immediately  
10 preceding instruction, said second comparator indicating whether  
11 said third operand register number of said current instruction  
12 matches said second destination register number of said immediately  
13 preceding instruction; and  
14 a second register file bypass multiplexer connected to  
15 said register file, said first functional unit group, said second  
16 functional unit group and said second comparator, said second  
17 register file bypass multiplexer having a first input receiving  
18 data from said register corresponding to said third operand  
19 register number of said current instruction, a second input  
20 connected to said output of said second functional unit group and  
21 an output supplying an operand to said operand input of said first  
22 functional unit group, said second multiplexer selecting said data  
23 from said register corresponding to said third operand number of  
24 said current instruction if said second comparator fails to  
25 indicate a match and selecting said output of said second  
26 functional unit group if said second comparator indicates a match.

1 7. (Previously Amended) The data processing apparatus of  
2 claim 6, said first comparator further receiving an indication of  
3 said first destination register of said immediately preceding  
4 instruction, said first comparator further indicating whether said  
5 first operand register number of said current instruction matches  
6 said first destination register number of said immediately  
7 preceding instruction, said first multiplexer further having a  
8 third input connected to said output of said first functional unit

9 group, said first multiplexer selecting said output of said first  
10 functional unit group if said first comparator indicates a match,  
11 said second comparator further receiving an indication of said  
12 first destination register of said immediately preceding  
13 instruction, said second comparator further indicating whether said  
14 third operand register number of said current instruction matches  
15 said first destination register number of said immediately  
16 preceding instruction, said second multiplexer further having a  
17 third input connected to said output of said first functional unit  
18 group, and said second multiplexer selecting said output of said  
19 first functional unit group if said second comparator indicates a  
20 match.

1 8. (Currently Amended) The data processing apparatus of claim  
2 1, further comprising:

3 a second comparator receiving an indication of said second  
4 operand register number of a current instruction and an indication  
5 of said second destination register number of an immediately  
6 preceding instruction, said second comparator indicating whether  
7 said second operand register number of said current instruction  
8 matches said second destination register number of said immediately  
9 preceding instruction; and

10 a second register file bypass multiplexer connected to said  
11 register file, said first functional unit group, said second  
12 functional unit group and said second comparator, said second  
13 register file bypass multiplexer having a first input receiving  
14 data from said register corresponding to said second operand  
15 register number of said current instruction, a second input  
16 connected to said output of said second functional unit group and  
17 an output supplying an operand to said operand input of said second  
18 functional unit group, said second multiplexer selecting said data  
19 from said register corresponding to said second operand number of

20 said current instruction if said second comparator fails to  
21 indicate a match and selecting said output of said second  
22 functional unit group if said second comparator indicates a match.

1 9. (Previously Amended) The data processing apparatus of  
2 claim 8, said second comparator further receiving an indication of  
3 said first destination register number of an immediately preceding  
4 instruction, said second comparator indicating whether said second  
5 operand register number of said current instruction matches said  
6 first destination register number of said immediately preceding  
7 instruction, said second multiplexer further having a third input  
8 connected to said output of said first functional unit group, and  
9 said second multiplexer further selecting said output of said first  
10 functional unit group if said second comparator indicates a match.

10. (Canceled)

1 11. (Currently Amended) A data processing apparatus  
2 comprising:  
3 a first register file comprising a plurality of registers,  
4 each of said plurality of registers having a corresponding register  
5 number;  
6 a second register file comprising a plurality of registers,  
7 each of said plurality of registers having a corresponding register  
8 number;  
9 a first functional unit group including an input connected to  
10 said first and second register files, an output connected to said  
11 first register file, ~~and~~ a plurality of first functional units each  
12 having an output, and an output multiplexer having a plurality of  
13 inputs receiving respective outputs of said first functional units  
14 and an output, said first functional unit group responsive to an  
15 instruction to

16           receive data from one of said plurality of registers in  
17           said first and second register files corresponding to an  
18           instruction-specified first operand register number at an  
19           operand input,

20           operate on said received data employing an instruction-  
21           specified one of said first functional units, and

22           select said output of said instruction-specified one of  
23           said first functional units via said output multiplexer, and

24           output data from said output of said output multiplexer to  
25           one of said plurality of registers in said first register file  
26           corresponding to an instruction-specified first destination  
27           register number from an output;

28           a second functional unit group including an input connected to  
29           said first and second register files, an output connected to said  
30           second register file, and a plurality of second functional units  
31           each having an output, and an output multiplexer having a plurality  
32           of inputs receiving respective outputs of said second functional  
33           units and an output, said second functional unit group responsive  
34           to an instruction to

35           receive data from one of said plurality of registers in  
36           said first and second register files corresponding to an  
37           instruction-specified second operand register number at an  
38           operand input,

39           operate on said received data employing an instruction-  
40           specified one of said second functional units, and

41           select said output of said instruction-specified one of  
42           said second functional units via said output multiplexer, and

43           output data from said output of said output multiplexer to  
44           one of said plurality of registers in said second register  
45           file corresponding to an instruction-specified second  
46           destination register number from an output; and



47 a first crosspath connecting said second register file to said  
48 first functional unit group comprising  
49 a first crosspath comparator, wherein, if said first  
50 operand register is in said second register file, said  
51 comparator receives an indication of said first operand  
52 register number of a current instruction and an indication of  
53 said second destination register number of a preceding  
54 instruction, and said first crosspath comparator indicates  
55 whether said first operand register number of said current  
56 instruction matches said second destination register number of  
57 said preceding instruction, and  
58 a first crosspath multiplexer connected to said second  
59 register file, said first functional unit group, said second  
60 functional unit group and said first crosspath comparator,  
61 said first crosspath multiplexer having a first input  
62 receiving data from said register corresponding to said first  
63 operand register number of said current instruction, a second  
64 input connected to said output of said second functional unit  
65 group and an output supplying an operand to said operand input  
66 of said first functional unit group, wherein, if said first  
67 operand register is in said second register file, said first  
68 crosspath multiplexer selects said data from said register  
69 corresponding to said first operand number of said current  
70 instruction if said first crosspath comparator fails to  
71 indicate a match and selects said output of said second  
72 functional unit group if said first crosspath comparator  
73 indicates a match;  
74 said first functional units of said first functional unit  
75 group and said second functional units of said second functional  
76 unit group selected whereby functions often executed simultaneously  
77 within the same instruction cycle have corresponding functional  
78 units placed in different functional unit groups and functions

79 which are not often executed together within the same instruction  
80 cycle have corresponding functional units placed in the same  
81 functional unit group.

12 to 17. (Canceled)

1 18. (Previously Added) The data processing apparatus of claim  
2 2, wherein:

3 each first functional unit of said first functional unit group  
4 and each second functional unit of said second functional unit group  
5 includes a pipeline latch in the middle for latching a logical state  
6 of said functional unit between said first pipeline stage and said  
7 second pipeline stage.

19. (Canceled)

1 20. (New) The data processing apparatus of claim 11, wherein  
2 said register file, said first functional unit group, said second  
3 functional unit group, said first comparator and said first  
4 register file bypass multiplexer operate according to an  
5 instruction pipeline comprising:

6 a first pipeline stage consisting of a register read operation  
7 from said register file to provide operands for a selected  
8 functional unit of said first and second functional unit groups and  
9 a first half of operation of a said selected functional unit of  
10 said first and said second functional unit groups, and

11 a second pipeline stage consisting of a second half of  
12 operation of said selected functional unit of said first and said  
13 second functional unit groups and a register write operation to  
14 said register file of results of operation of said selected  
15 functional unit of said first and second functional unit groups,

16        wherein the sum of the time of said register read operation  
17        and said register write operation equals approximately the sum of  
18        the time of said first and second halves of operation of a slowest  
19        of said functional units of said first and second functional unit  
20        groups.

1        21. (New) The data processing apparatus of claim 20, wherein:  
2        each first functional unit of said first functional unit group  
3        and each second functional unit of said second functional unit group  
4        includes a pipeline latch in the middle for latching a logical state  
5        of said functional unit between said first pipeline stage and said  
6        second pipeline stage.

1        22. (New) The data processing apparatus of claim 11, further  
2        comprising an output register having an input connected to said  
3        output of said second functional unit group and an output connected  
4        to said register file for temporarily storing said output of said  
5        second functional unit group prior to storing in said register  
6        corresponding to said second destination register number,  
7        wherein said first comparator further receives an indication  
8        of said second destination register number of a second preceding  
9        instruction, said first comparator further indicating whether said  
10       first operand register number of said current instruction matches  
11       said second destination register number of said second preceding  
12       instruction, and  
13       wherein said multiplexer further has a third input connected  
14       to said output register output, said multiplexer selecting said  
15       output register output if said first comparator indicates a match.

1        23. (New) The data processing apparatus of claim 11, said  
2        first comparator further receiving an indication of said first  
3        destination register of said immediately preceding instruction,

4 said first comparator further indicating whether said first operand  
5 register number of said current instruction matches said first  
6 destination register number of said immediately preceding  
7 instruction, said first multiplexer further having a third input  
8 connected to said output of said first functional unit group, and  
9 said first multiplexer selecting said ~~first~~ output of said first  
10 functional unit group if said first comparator indicates a match.

1        24. (New) The data processing apparatus of claim 11, said  
2 first functional unit group further responsive to an instruction to  
3 receive data from one of said plurality of registers corresponding  
4 to an instruction-specified third operand register number at an  
5 operand input,  
6        said apparatus further comprising:  
7        a second comparator receiving an indication of said third  
8 operand register number of a current instruction and an indication  
9 of said second destination register number of said immediately  
10 preceding instruction, said second comparator indicating whether  
11 said third operand register number of said current instruction  
12 matches said second destination register number of said immediately  
13 preceding instruction; and  
14        a second register file bypass multiplexer connected to  
15 said register file, said first functional unit group, said second  
16 functional unit group and said second comparator, said second  
17 register file bypass multiplexer having a first input receiving  
18 data from said register corresponding to said third operand  
19 register number of said current instruction, a second input  
20 connected to said output of said second functional unit group and  
21 an output supplying an operand to said operand input of said first  
22 functional unit group, said second multiplexer selecting said data  
23 from said register corresponding to said third operand number of  
24 said current instruction if said second comparator fails to

25 indicate a match and selecting said output of said second  
26 functional unit group if said second comparator indicates a match.

1        25. (New) The data processing apparatus of claim 24, said  
2 first comparator further receiving an indication of said first  
3 destination register of said immediately preceding instruction,  
4 said first comparator further indicating whether said first operand  
5 register number of said current instruction matches said first  
6 destination register number of said immediately preceding  
7 instruction, said first multiplexer further having a third input  
8 connected to said output of said first functional unit group, said  
9 first multiplexer selecting said output of said first functional  
10 unit group if said first comparator indicates a match,  
11        said second comparator further receiving an indication of said  
12 first destination register of said immediately preceding  
13 instruction, said second comparator further indicating whether said  
14 third operand register number of said current instruction matches  
15 said first destination register number of said immediately  
16 preceding instruction, said second multiplexer further having a  
17 third input connected to said output of said first functional unit  
18 group, and said second multiplexer selecting said output of said  
19 first functional unit group if said second comparator indicates a  
20 match.

1        26. (New) The data processing apparatus of claim 11, further  
2 comprising:

3        a second comparator receiving an indication of said second  
4 operand register number of a current instruction and an indication  
5 of said second destination register number of an immediately  
6 preceding instruction, said second comparator indicating whether  
7 said second operand register number of said current instruction

8 matches said second destination register number of said immediately  
9 preceding instruction; and  
10 a second register file bypass multiplexer connected to said  
11 register file, said first functional unit group, said second  
12 functional unit group and said second comparator, said second  
13 register file bypass multiplexer having a first input receiving  
14 data from said register corresponding to said second operand  
15 register number of said current instruction, a second input  
16 connected to said output of said second functional unit group and  
17 an output supplying an operand to said operand input of said second  
18 functional unit group, said second multiplexer selecting said data  
19 from said register corresponding to said second operand number of  
20 said current instruction if said second comparator fails to  
21 indicate a match and selecting said output of said second  
22 functional unit group if said second comparator indicates a match.

1 27. (New) The data processing apparatus of claim 26, said  
2 second comparator further receiving an indication of said first  
3 destination register number of an immediately preceding  
4 instruction, said second comparator indicating whether said second  
5 operand register number of said current instruction matches said  
6 first destination register number of said immediately preceding  
7 instruction, said second multiplexer further having a third input  
8 connected to said output of said first functional unit group, and  
9 said second multiplexer further selecting said output of said first  
10 functional unit group if said second comparator indicates a match.

1 28. (New) A data processing apparatus comprising:  
2 a register file comprising a plurality of registers, each of  
3 said plurality of registers having a corresponding register number;

4        a first functional unit group connected to said register file  
5        and including a plurality of first functional units, said first  
6        functional unit group responsive to an instruction to  
7        receive data from one of said plurality of registers  
8        corresponding to an instruction-specified first operand  
9        register number at an operand input,  
10       operate on said received data employing an instruction-  
11       specified one of said first functional units, and  
12       output data to one of said plurality of registers  
13       corresponding to an instruction-specified first destination  
14       register number from an output;  
15       a second functional unit group connected to said register file  
16       and including a plurality of second functional units, said second  
17       functional unit group responsive to an instruction to  
18       receive data from one of said plurality of registers  
19       corresponding to an instruction-specified second operand  
20       register number at an operand input,  
21       operate on said received data employing an instruction-  
22       specified one of said second functional units, and  
23       output data to one of said plurality of registers  
24       corresponding to an instruction-specified second destination  
25       register number from an output;  
26       a first comparator receiving an indication of said first  
27       operand register number of a current instruction and an indication  
28       of said second destination register number of an immediately  
29       preceding instruction, said first comparator indicating whether  
30       said first operand register number of said current instruction  
31       matches said second destination register number of said immediately  
32       preceding instruction; and  
33       a first register file bypass multiplexer connected to said  
34       register file, said first functional unit group, said second  
35       functional unit group and said first comparator, said first

36 register file bypass multiplexer having a first input receiving  
37 data from said register corresponding to said first operand  
38 register number of said current instruction, a second input  
39 connected to said output of said second functional unit group and  
40 an output supplying an operand to said operand input of said first  
41 functional unit group, said first multiplexer selecting said data  
42 from said register corresponding to said first operand number of  
43 said current instruction if said first comparator fails to indicate  
44 a match and selecting said output of said second functional unit  
45 group if said first comparator indicates a match;

46       said first functional units of said first functional unit  
47 group and said second functional units of said second functional  
48 unit group selected whereby functions often executed simultaneously  
49 within the same instruction cycle have corresponding functional  
50 units placed in different functional unit groups and functions  
51 which are not often executed together within the same instruction  
52 cycle have corresponding functional units placed in the same  
53 functional unit group; and

54       wherein said register file, said first functional unit group,  
55 said second functional unit group, said first comparator and said  
56 first register file bypass multiplexer operate according to an  
57 instruction pipeline comprising:

58       a first pipeline stage consisting of a register read operation  
59 from said register file to provide operands for a selected  
60 functional unit of said first and second functional unit groups and  
61 a first half of operation of said selected functional unit of said  
62 first and said second functional unit groups, and

63       a second pipeline stage consisting of a second half of  
64 operation of said selected functional unit of said first and said  
65 second functional unit groups and a register write operation to  
66 said register file of results of operation of said selected  
67 functional unit of said first and second functional unit groups,



68 wherein the sum of the time of said register read operation  
69 and said register write operation equals approximately the sum of  
70 the time of said first and second halves of operation of a slowest  
71 of said functional units of said first and second functional unit  
72 groups.

1 29. (New) The data processing apparatus of claim 28, further  
2 comprising an output register having an input connected to said  
3 output of said second functional unit group and an output connected  
4 to said register file for temporarily storing said output of said  
5 second functional unit group prior to storing in said register  
6 corresponding to said second destination register number,

7 wherein said first comparator further receives an indication  
8 of said second destination register number of a second preceding  
9 instruction, said first comparator further indicating whether said  
10 first operand register number of said current instruction matches  
11 said second destination register number of said second preceding  
12 instruction, and

13 wherein said multiplexer further has a third input connected  
14 to said output register output, said multiplexer selecting said  
15 output register output if said first comparator indicates a match.

1 30. (New) The data processing apparatus of claim 28, said  
2 first comparator further receiving an indication of said first  
3 destination register of said immediately preceding instruction,  
4 said first comparator further indicating whether said first operand  
5 register number of said current instruction matches said first  
6 destination register number of said immediately preceding  
7 instruction, said first multiplexer further having a third input  
8 connected to said output of said first functional unit group, and  
9 said first multiplexer selecting said ~~first~~ output of said first  
10 functional unit group if said first comparator indicates a match.

1        31. (New) The data processing apparatus of claim 28, said  
2 first functional unit group further responsive to an instruction to  
3 receive data from one of said plurality of registers corresponding  
4 to an instruction-specified third operand register number at an  
5 operand input,

6        said apparatus further comprising:

7            a second comparator receiving an indication of said third  
8 operand register number of a current instruction and an indication  
9 of said second destination register number of said immediately  
10 preceding instruction, said second comparator indicating whether  
11 said third operand register number of said current instruction  
12 matches said second destination register number of said immediately  
13 preceding instruction; and

14           a second register file bypass multiplexer connected to  
15 said register file, said first functional unit group, said second  
16 functional unit group and said second comparator, said second  
17 register file bypass multiplexer having a first input receiving  
18 data from said register corresponding to said third operand  
19 register number of said current instruction, a second input  
20 connected to said output of said second functional unit group and  
21 an output supplying an operand to said operand input of said first  
22 functional unit group, said second multiplexer selecting said data  
23 from said register corresponding to said third operand number of  
24 said current instruction if said second comparator fails to  
25 indicate a match and selecting said output of said second  
26 functional unit group if said second comparator indicates a match.

1        32. (New) The data processing apparatus of claim 31, said  
2 first comparator further receiving an indication of said first  
3 destination register of said immediately preceding instruction,  
4 said first comparator further indicating whether said first operand

5 register number of said current instruction matches said first  
6 destination register number of said immediately preceding  
7 instruction, said first multiplexer further having a third input  
8 connected to said output of said first functional unit group, said  
9 first multiplexer selecting said output of said first functional  
10 unit group if said first comparator indicates a match,  
11 said second comparator further receiving an indication of said  
12 first destination register of said immediately preceding  
13 instruction, said second comparator further indicating whether said  
14 third operand register number of said current instruction matches  
15 said first destination register number of said immediately  
16 preceding instruction, said second multiplexer further having a  
17 third input connected to said output of said first functional unit  
18 group, and said second multiplexer selecting said output of said  
19 first functional unit group if said second comparator indicates a  
20 match.

1 33. (New) The data processing apparatus of claim 28, further  
2 comprising:  
3 a second comparator receiving an indication of said second  
4 operand register number of a current instruction and an indication  
5 of said second destination register number of an immediately  
6 preceding instruction, said second comparator indicating whether  
7 said second operand register number of said current instruction  
8 matches said second destination register number of said immediately  
9 preceding instruction; and  
10 a second register file bypass multiplexer connected to said  
11 register file, said first functional unit group, said second  
12 functional unit group and said second comparator, said second  
13 register file bypass multiplexer having a first input receiving  
14 data from said register corresponding to said second operand  
15 register number of said current instruction, a second input

16 connected to said output of said second functional unit group and  
17 an output supplying an operand to said operand input of said second  
18 functional unit group, said second multiplexer selecting said data  
19 from said register corresponding to said second operand number of  
20 said current instruction if said second comparator fails to  
21 indicate a match and selecting said output of said second  
22 functional unit group if said second comparator indicates a match.

1 34. (New) The data processing apparatus of claim 33, said  
2 second comparator further receiving an indication of said first  
3 destination register number of an immediately preceding  
4 instruction, said second comparator indicating whether said second  
5 operand register number of said current instruction matches said  
6 first destination register number of said immediately preceding  
7 instruction, said second multiplexer further having a third input  
8 connected to said output of said first functional unit group, and  
9 said second multiplexer further selecting said output of said first  
10 functional unit group if said second comparator indicates a match.

1 35. (New) The data processing apparatus of claim 28, wherein:  
2 each first functional unit of said first functional unit group  
3 and each second functional unit of said second functional unit group  
4 includes a pipeline latch in the middle for latching a logical state  
5 of said functional unit between said first pipeline stage and said  
6 second pipeline stage.